IN THE CLAIMS:

1. (currently amended): A semiconductor device, comprising:

a first semiconductor chip that includes a first main surface, a second main surface which is located on the reverse side of the first main surface and whose surface area is larger than that of the first main surface, and a side wall surface that connects between the first and second main surfaces;

a first pad provided on the first main surface of the first semiconductor chip;

a semiconductor chip carrying portion that includes a third main surface which faces the second main surface of the first semiconductor chip and which has a first region and a second region that surrounds the first region, and a fourth main surface which is located on the reverse side of the third main surface;

a first wiring layer which is electrically connected to the first pad and which extends from the first pad, along the first main surface and the side wall surface, to above the second region;

an external terminal which is provided over the second region and electrically connected to the first pad via the first wiring layer; and

a post portion, which is provided ~~between~~ on the first wiring layer ~~and the external terminal~~.

2. (original): The semiconductor device according to claim 1, further comprising a conductive portion formed in a through hole that penetrates from the third main surface to the fourth main surface, and the conductive portion being electrically connected to the first wiring layer.

3. (original): The semiconductor device according to claim 1, further comprising a wiring portion provided on the third main surface of the semiconductor chip carrying portion and transecting the second main surface and electrically connected to the first wiring layer; and

a first pad electrically connected to the external terminal via the first wiring layer and the wiring portion.

4. (original): The semiconductor device according to claim 1,

wherein the semiconductor chip carrying portion is a second semiconductor chip having a second pad electrically connected to the first wiring layer.

5. (original): The semiconductor device according to claim 1,

wherein the semiconductor chip carrying portion is a second semiconductor chip, the semiconductor device further comprising a second wiring layer provided between the first semiconductor chip and the second semiconductor chip and transecting the second main surface and electrically connected to the first wiring layer, and wherein the first pad is electrically connected to the external terminal via the first wiring layer and the second wiring layer.

6. (currently amended): The semiconductor device according to claim 1, further comprising:

wherein the post portion is provided between the first wiring layer and the external terminal; and

a sealing layer provided on the first wiring layer and on the side surface of the post portion.

7. (original): The semiconductor device according to claim 6, wherein an oxidation film is formed on a side surface of the post portion.

8. (original): The semiconductor device according to claim 1, wherein the width of a part of the first wiring layer which is located above the boundary between the first main surface and the side wall surface is formed wider than the remaining parts of the first wiring layer.

9. (original): The semiconductor device according to claim 1, wherein a plurality of chips are stacked.

10.-21. (canceled)